IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of

Applicant	:	Patrick W. Tandy
Serial No.	:	10/804,952
Filed	:	March 19, 2004
Title	:	**METHOD OF FORMING A NON-CONTINUOUS CONDUCTIVE LAYER FOR LAMINATED SUBSTRATES**
Docket	:	MIO0048V2/40509.295
Examiner	:	M. Trinh
Art Unit	:	3729
Conf. No.	:	8084

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Commissioner for Patents
P.O. Box 1450
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Sir:

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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Applicant requests review of the final rejection mailed August 3, 2006, in the above-identified application pursuant to the Program announced at 1296 OG 67 (July 12, 2005). No amendments are being filed with this Request. This Request is being filed with a Notice of Appeal. Review by a panel of examiners is requested for the reasons stated below.

The present status of claims is: claims 1-8 stand withdrawn from consideration based on a previous restriction requirement; claims 9-10 stand rejected; and claims 11-15 have been objected to, but have been indicated to be allowable if re-written in independent form. In the Final Rejection, the Examiner stated two grounds of rejection: claims 9-10 were rejected under 35 USC §103 as unpatentable over the "Admitted Prior Art" depicted in applicant's drawing Figs. 1 and 2; and, claims 9-10 were rejected under 35 USC §103 as unpatentable over Tsukamoto (US 5841194) in view of the "Admitted Prior Art." Applicant filed an Amendment After Final Rejection on October 2, 2006. The Examiner issued an Advisory Action on October 13, 2006, stating that the Amendment was refused entry.

Applicant submits that the rejections are not well taken in that: clear errors of fact have been made and clear deficiencies exist in the record with respect to motivation or suggestion to combine the reference teachings. Applicant will discuss each error in detail below.

The Examiner's assertions regarding the "Admitted Prior Art" directly contradict applicant's explicit disclosure and claim language.

In the final rejection (page 2) the Examiner asserted that the "APA" showed "forming a first layer of conductive material over an insulating layer" and "removing portions of said conductive material of said first layer to define a first circuit pattern and a first rail area that is electrically isolated from said first circuit pattern." Applicant agrees that Prior Art Fig. 2 shows the formation of a circuit pattern 204 and a first rail 201 by removal of conductive material around the circuit pattern and between the circuit pattern and the rail. Applicant also agrees that conductive pattern 204 and first rail 201 are electrically isolated.

However, the Examiner then went on to assert that "APA inherently discloses the removing portions of said conductive material of said first layer *from said first rail area*."[Emphasis supplied.] Applicant submits that that assertion is factually incorrect and directly contradicts the written description found at page 7, paragraph [0027] where it is stated that:

> As stated earlier, figure 2 is an example of a standard circuit board 200 used for memory devices such as dual in line memory modules (DIMMs). The circuit board includes a first rail 201, a second rail 202, a number of sites 203 and a patterned area 204. A rail is an area along the edge of a circuit board. The rails 201 and 202 do not generally contain conductive paths, bonding pads or the like. *Thus, the rails 201 and 202 do not get etched and conductive material is not removed from the rails 201 and 202.* The rails 201 and 202 include a large amount of conductive material such as copper. *The conductive material stretches from one end of the substrate to the other.* ... The circuit board 200 of figure 2 is susceptible to deformation and warping due to expansion and contraction of the circuit board during thermal cycling. This circuit board has a tendency to remember any deformation that it is subjected to and can cause errors in processing. [Emphasis supplied.]

As can be seen, the specification explicitly states that ***no*** portions of the conductive material are removed from the rails 201 and 202. The Examiner is simply wrong in his assertions, and a clear factual error has been made.

Applicant's claim 9 recites, *inter alia*, "removing portions of said conductive material of said first layer *from said first rail area* such that no continuous lengths of conductive material remain *within said first rail area*."[Emphasis supplied.] As taught at page 7, paragraphs [0028] and [0029], the claimed invention *differs* from the prior art in the removal of at least a portion of the conductive material from the rail areas so that the resulting circuit pattern has a reduced tendency to warp or deform.

As can be seen, the basis for the rejection is the Examiner's incorrect understanding of Prior Art Fig. 2 and the accompanying description of that circuit board. Nothing in Prior Art Fig. 2, or the accompanying description, teaches or suggests the claimed subject matter. The rejection is not well taken and should be withdrawn.

Tsukamoto taken with "APA" does not teach or suggest the claimed subject matter.

While claims 9 and 10 clearly recite that they are directed to a method of fabricating a circuit board, Tsukamoto has little relevance to the fabrication of a circuit board. Rather, Tsukamoto depicts a chip carrier for packaging a semiconductor chip device comprising an insulating board substrate 101 having a peripheral stiffener 106. A semiconductor chip 201 (already fabricated) is designed to be inserted into the carrier such that bonding pads on the chip carrier match up with terminal electrodes on the underside of the mounted chip. Tsukamoto contains absolutely no description that conductive material is removed from the pre-fabricated chip. Nor does Tsukamoto contain any description whatsoever that any conductive material has been removed from the carrier.

Tsukamoto is so far removed in method of fabrication, structure and operation from applicant's invention that it has been difficult for applicant to follow the Examiner's reasoning. The Examiner asserted in the final rejection (page 3) that "Tsukamoto however inherently discloses the removing portions of said conductive material 102 of said first layer ..."

What Tsukamoto clearly describes is that element 102 is a "bonding pad." Tsukamoto does *not* describe how such bonding pad came to be formed. It appears that the Examiner has been equating one of the bond pads 102 as a "circuit pattern" (which it clearly is not) and another of the bond pads 102 as a "rail area" (which it clearly is not). The only circuitry described by Tsukamoto is on the semiconductor chip 201. There is no teaching in Tsukamoto of "removing portions of said conductive material of said first layer to define a first circuit pattern" as recited in claim 9. Applicant expressly disputes that the bond pads 102 of Tsukamoto can properly be considered to be either a "circuit pattern" or a "rail area." Tsukamoto is silent concerning how bond pads 102 are formed. Silence in a reference does not form a basis for a conclusion of obviousness.

Nor is removal of conductive material "inherent" in Tsukamoto as the Examiner asserts. Bond pads 102 could just as likely have been formed using a removable mask so that conductive material is deposited only on specific areas of insulating board 101. In order for the Examiner to rely upon inherency in a reference, the *Examiner* bears the burden of proof that the asserted feature must *necessarily and always* be formed in the manner asserted. MPEP, §2112. Here, the Examiner has failed to carry that evidentiary burden. The Examiner has failed to point to *any* teaching in Tsukamoto that would prove that bond pads 102 are formed in the manner speculated by the Examiner. The rejection fails for this reason alone.

Moreover, Tsukamoto fails to teach or suggest "removing portions of said conductive material ... from said first rail area" as recited in claim 9. The Examiner asserted in the final rejection (page 3) that Tsukamoto taught the removal of "portions of said conductive material of said first layer from said first rail area," and justified this assertion by reference to "see Fig. 1, depicts rail area and mounting pad." The Examiner has never clearly described which element in Fig. 1 of Tsukamoto comprises the "rail area." Assuming again that the Examiner is asserting that at least one of bond pads 102 (incredibly making alternate ones of the *same* bond pads serve as *both* circuit patterns and rail areas) corresponds to the recited "first rail area," nothing in Tsukamoto teaches or suggest removing any material whatsoever from bond pads 102. In order to support the Examiner's reasoning, Tsukamoto would have to form a bond pad 102 and then remove at least a portion of the conductive material making up bond pad 102. It is quite clear that Tsukamoto fails to even hint at such a fabrication step.

The Examiner then further argues in the final rejection (page 3) that it would have been obvious "to employ the APA's teaching of removing portions of said conductive material ... from said first rail area." As discussed above, that assertion is factually incorrect. Nor has the Examiner provided any evidence or reasoning to support the proposed combination of Tsukamoto, who has nothing to do with fabrication of a circuit board, with the "APA." And, as previously quoted above, paragraph [0027] of applicant's disclosure explicitly states with respect to Prior Art Fig. 2 that no conductive material is removed from the rail area and that the rail areas "do not generally contain conductive paths bonding pads, or the like." The Examiner has provided no basis for the proposed combination. Claims 9 and 10 are patentable over Tsukamoto and "APA".

Conclusion

For all of the above reasons, applicant submits that claims 9-10 are patentable over the "Admitted Prior Art" and Tsukamoto. Claims 11-15 were previously indicated to contain allowable subject matter. Accordingly, applicant respectfully requests the withdrawal of all grounds of rejection and the allowance of claims 9-15.

Respectfully submitted,
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